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Application of synopsys' taurus TCAD in developing CMOS fabrication process modules

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Abstract

Technology CAD (TCAD) refers to the use of computer simulation to model semiconductor processing and device operation. TCAD has two major functions namely process simulation and device simulation. It performs the semiconductor process simulation and the device simulation by taking the description of the transistor layout input to simulate the fabrication process and device behavior before the actual silicon is made. This paper illustrates the use of Synopsys' Taurus TCAD to develop and simulate the fabrication and electrical behavior of NMOS and PMOS transistors in the complete CMOS process flow. Illustration also includes how mask information extracted from a layout by Taurus Layout is used by TSUPREM-4 to produce an output file containing complete structure, mesh and doping information that can be read into MEDICI device simulator to extract electrical characteristics. The specified process includes, not only steps required to simulate a MOSFET device, but also all steps of the hypothetical CMOS process.

1. Introduction

This paper demonstrates the application of Taurus TCAD, developed by Synopsys, in the development of CMOS fabrication process modules in UniMAP [1, 2, 3]. However, the discussions of the content focus on the development and simulation of NMOS and PMOS transistors in a complete CMOS process flow. The main goal of the simulation is to obtain two-dimensional device structure with doping profiles and its current-voltage characteristics.

Modeling of technological processes is increasingly attractive to the semiconductor industry [4,5]. First, it can save time. Second, it can reduce processing costs of silicon wafers. A semiconductor fab acts as a computer that may need a few months to run a batch. Simulation can give results within a few days, so virtual experiments would be optimal.

The use of technology computer aided design (TCAD) is an important tool to simulate the actual wafer fabrication process and device characterization [5,12]. This enables engineers to obtain realistic device structures, process information such as doping profiles,

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layer thickness through process simulation and electrical information such as I-V and C-V characteristics through 2D device simulation before the transistor is fabricated [6,7]. With TCAD, optimum device performance can be achieved from process variations. This greatly aids in the development and understanding of the semiconductor process and device operation.

2. Methodology

2(a) Taurus TCAD

Before reviewing the simulation of CMOS, a brief introduction to Taurus TCAD must be presented. Taurus TCAD is a powerful simulation and modeling application suite. It combines the Taurus Modeling Environment (TME) and a variety of simulators to simulate designs. TME is a unified scripting infrastructure that combines Taurus Visual, Taurus Workbench, and Taurus Layout. In Taurus TCAD, Taurus TSUPREM-4 and Taurus MEDICI are two simulation programs used to perform process simulation and device simulation.

2(b) Process Simulation

Process simulation involves modeling all essential steps in the process flow in order to obtain dopant and stress profiles and, to a lesser extent, device geometry. The input for process simulation is the process flow and a layout. The layout is selected as a linear cut in a full layout for a 2D simulation or a rectangular cut from the layout for a 3D simulation [5,9].

The layout of CMOS is created using Taurus Layout mask editor. The mask layout of CMOS consists of five mask layers namely nwell, active, gate, contact and metal. Mask nwell is used to define the n+ well for the PMOS transistor in the p-type substrate. It is represented in yellow. Mask active is used to create the source and drain of a transistor. It is green in color. Mask gate is for the gate definition and it is represented in red. Mask contact defines the holes for contact between metal and substrate. Mask metal is a blue layer that defines the metal contacts on the transistors. Figure 1 shows the completed mask layout of 2μm N-Well CMOS.

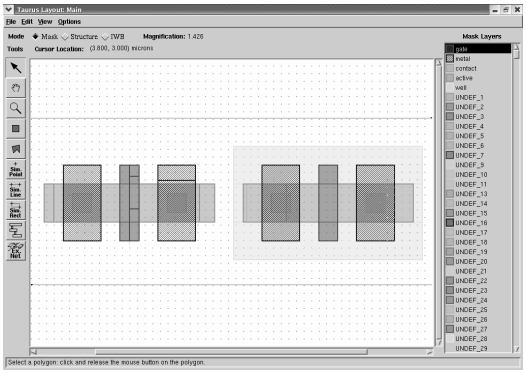

Fig. 1: Mask layout of CMOS

Once the layout is finished, it is saved twice, once in TL2 format and once in TL1 format. The TL2 format saves the whole mask layout while the TL1 format saves the one-dimensional cutline of the mask layout. The cutline is used to define the area on the mask to be simulated at lithography steps in the process flow during process simulation.

The fabrication of CMOS requires a series processing steps called a process flow [8,11]. In Taurus TCAD, the process flow is described inside Taurus WorkBench Experiment window created to build up the process modules and recipes of the CMOS fabrication process. The process modules start with initial processing of the substrate wafer, followed by photolithography and ion implantations. All the processing steps are repeated until the final structure is obtained. Once the process simulation is done, the fabricated CMOS is passed to MEDICI for electrical characterization. Figure 2 summarizes the discussion.

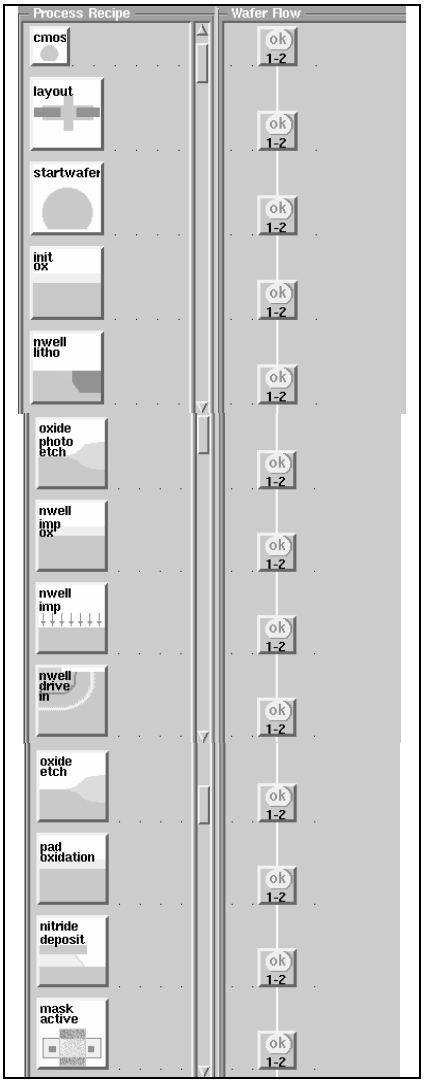

Fig. 2: Taurus WorkBench Experiment window

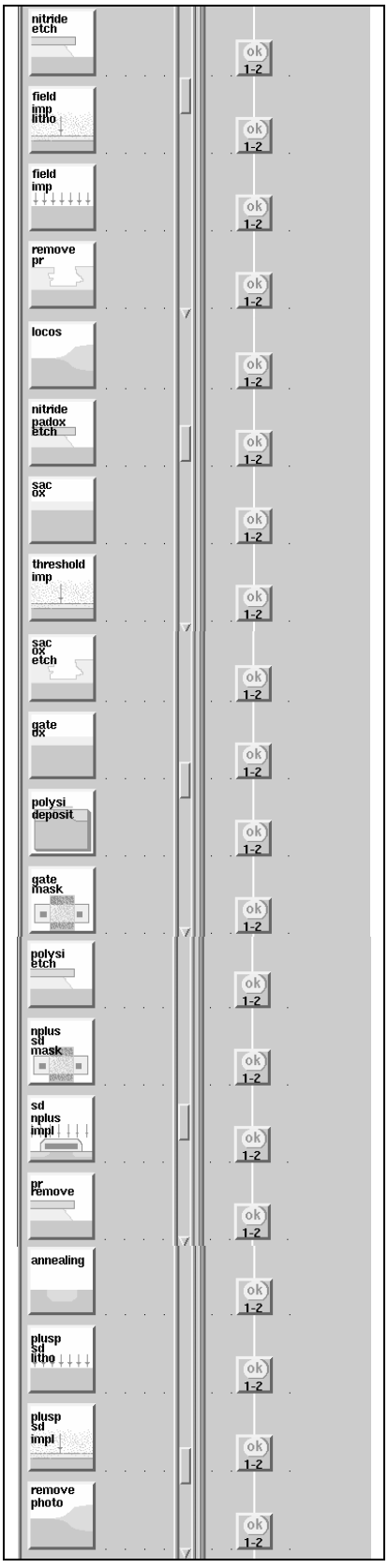

Fig. 2: continued

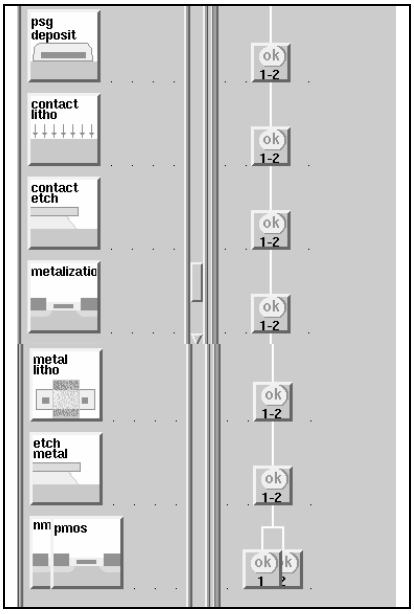

Fig. 2: continued

2(c) Device Simulation

Device simulation is the modeling of semiconductor electrical operation [10]. MEDICI is a device simulation program used to analyze the I-V characteristics and the threshold voltage of the transistors. Two experiments are created to build up the modules for device simulation. Each of the experiment simulates the I-V characteristics and the threshold voltage of NMOS and PMOS transistors respectively. The areas of device simulation are the gate characteristics, drain characteristics and the MOS parameter extraction. Figure 3 and 4 depicts the experiments set-up.

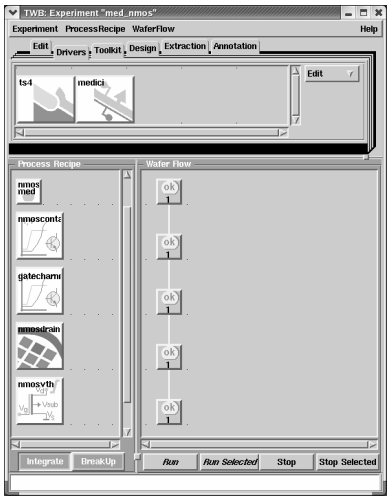

Fig. 3: NMOS Experiment

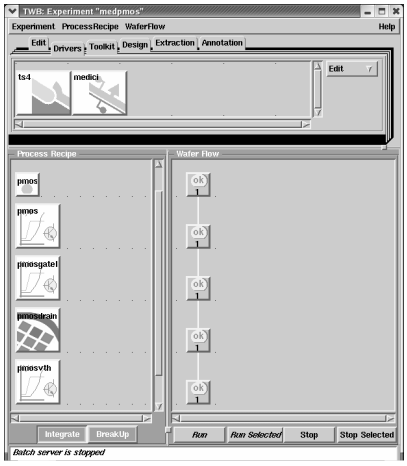

Fig. 4: PMOS Experiment

3. Results and discussion

3.1 Final Cross Section Results

The final simulation result obtained from process simulation is the two-dimensional device structure with grid information and doping profiles. Figure 5 shows the final cross section results of three different structures.

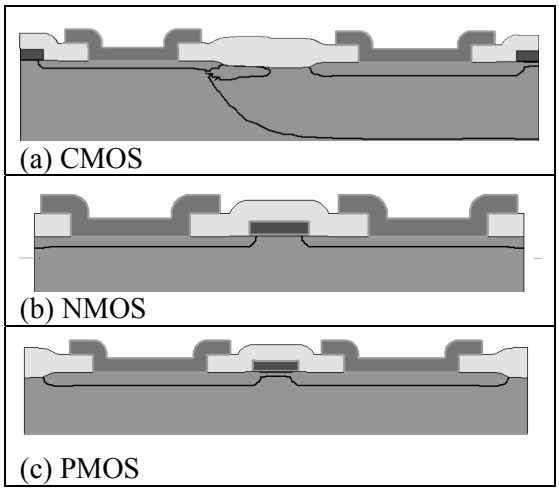

Fig. 5: Final Cross Section Results

The structure layers are represented by colors. Yellow represents the oxide, red for polysilicon, green for silicon substrate and blue represents the metal. The line in the each structure shows the junction depth of doping profiles.

3.2 Impurity Implantation Profiles

Figure 6 illustrates the effect of the ion implantation and drive in process on the phosphorus profile in the PMOS transistor.

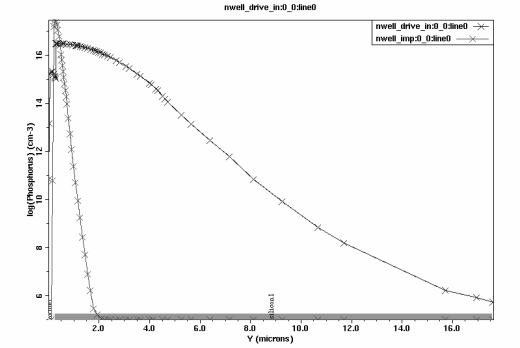

Fig. 6: Phosphorus Implantation and Drive in profiles for the N-Well.

Figure 7 compares the effect of ion implantation and annealing process on the arsenic profile in the NMOS transistor.

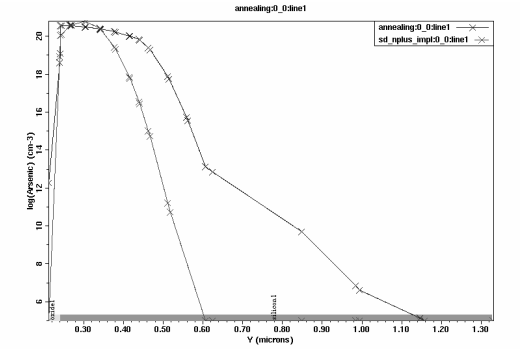

Fig. 7: Arsenic Implantation and Annealing profiles for the source and drain in the NMOS transistor.

Figure 8 shows the effect of ion implantation on the boron profile for the source and drain in the PMOS transistor.

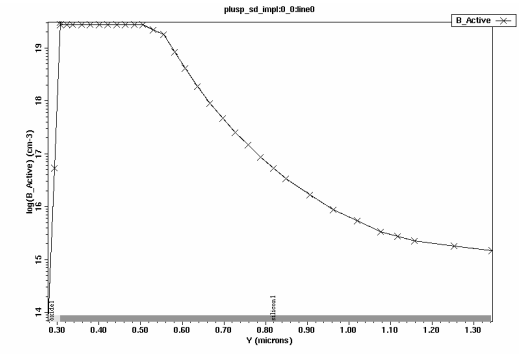

Fig. 8: Boron Implantation profile for the source and drain in the PMOS transistor.

3.3 I-V Characteristics

An I-V curve analysis is performed for gate bias of 3V and drain biases from 0V to 3V for NMOS transistor while drain biases from 0V to -3V for PMOS transistor. Figure 9 and 10 illustrate the working operation of the NMOS transistor and PMOS transistor in the enhancement mode.

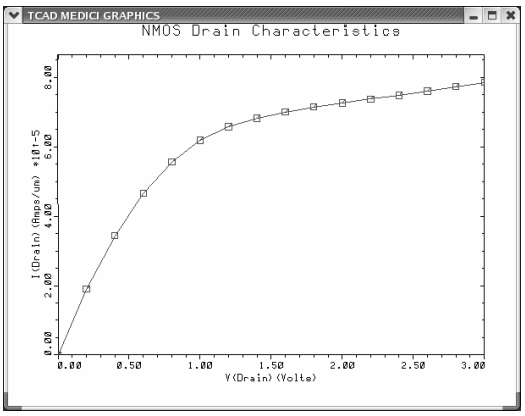

Fig. 9: NMOS I_d-V_{ds} Curve

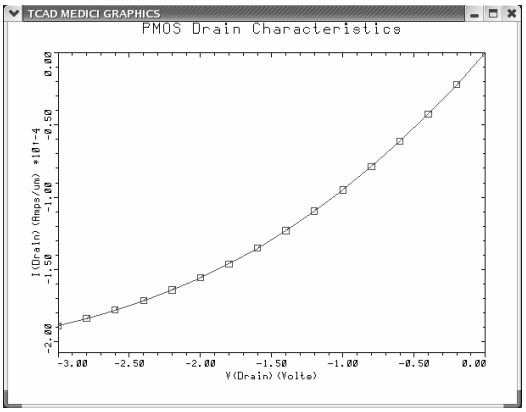

Fig. 10: PMOS I_d-V_{ds} Curve

3.4 Threshold Voltage

The threshold voltage of operation of the device is determined from the plot of the drain source current voltage versus the gate voltage. The value is determined by extrapolation of the curve from the point of maximum slope to the x-axis intercept. The theoretical equation (1) for the threshold voltage of an ideal NMOS device is given by [9,11]

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_{sq} N_a (2\phi_F + V_{SB})}}{C_{ox}} \tag{1}$$

In Taurus TCAD, the threshold voltage is determined by I-V curve analysis and MOS parameter extraction. Figure 11 and 12 illustrate the drain source current voltage versus the gate voltage of NMOS transistor and PMOS transistor.

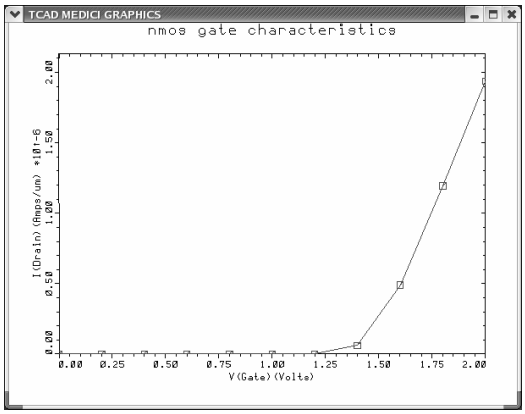

Fig. 11: NMOS I_d-V_{gs} Curve

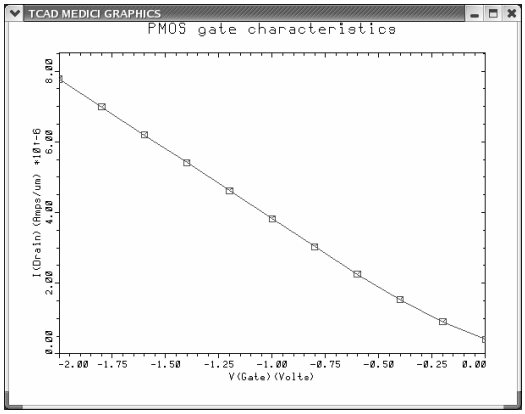

Fig. 12: PMOS I_d-V_{gs} Curve

The threshold voltage for the NMOS transistor and the PMOS transistor is 1.51V and – 0.167V.

4. Conclusion

This paper demonstrated the application of Synopsys' Taurus TCAD particularly the process and device simulation programs, TSUPREM-4 and MEDICI, to the development of CMOS fabrication process modules in KUKUM. Such project developed in KUKUM helps to gear towards the fabrication of first CMOS wafers in Microfabrication Clean room.

Acknowledgments

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